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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/954,637	09/14/2001	Christophe Lauga	851963.402	6886

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EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2133	6

DATE MAILED: 01/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/954,637	Applicant(s) LAUGA, CHRISTOPHE	
	Examiner James C Kerveros	Art Unit 2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 April 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 September 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Drawings

The drawings are objected to because in Figure 4, numeral 2, functional block is missing descriptive legends, thus requiring the reader to refer back to the specification. Suitable descriptive legends may be used subject to approval by the Office, or may be required by the examiner where necessary for understanding of the drawing. They should contain as few words as possible.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the claimed features "switch" and "switching arrangement," recited in claims 2 and 5 must be shown or the features canceled from the claims. No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3 and 5-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Motika et al. (US 5983380), issued: November 9, 1999.

Regarding Claim 1, Motika discloses a semiconductor integrated circuit device under test (DUT) 14 having a test scan arrangement, Figures 1 and 2, comprising:

A plurality of scan chains (128, 130, 132, 134, 136) each having an input end and an output end and being arranged in pairs (128, 130) as first scan chain (128) and a second scan chain (130).

A plurality of first terminals corresponding to scan 128 and second terminals corresponding to scan 130, from the shift register inputs (SRIs) for loading patterns into the chip's shift register latches (SRLs) generated by the tester externally to the DUT 14.

Compression logic multiple input signature register (MISR) 16 having a plurality of inputs and one output, where the plurality of inputs are connected to the output ends of the plurality of scan chains (128, 130, 132, 134, 136), and where the output is connected to the compression logic output terminal of the semiconductor integrated circuit (14) for external connection, as a (SIGNAL OUT) Figure 2.

The plurality of first terminals corresponding to scan (128) is connected to the input end of the first scan chain scan (128) of pair (128, 130) for external input connection.

The plurality of second terminals corresponding to scan 130 is selectively connected with ("mode select" signal of select register 142), which allows for a first state or a second state corresponding to (normal LSSD) or (WRPLBIST test mode). Wherein during the first state, the second terminal is connected to the input end of the second

scan chain (130) for external input connection and further, wherein during the second state, the second terminal is connected to the output end of the second scan chain (130) for external output connection, Figure 2.

The input end of the second scan chain (130) of pair (128, 130) is selectively connectable, with "mode select" signal from a mode select register 142 in the second state (WRPLBIST test mode), to the output end of the first scan chain (128) of each pair.

Regarding Claim 2, Motika discloses a switch (a "mode select" signal of select register 142), associated with scan chain pair (128, 130) for selectively connecting the input end of the second scan chain (130) to the output end of the first scan chain (128).

Regarding Claim 3, Motika discloses a plurality of multiplexers (2:1 MUX) associated with scan chain pair (128, 130), and having a first multiplexer input "0", also shown in detailed by Figure 3, connected to the output end of the first scan chain (128), a second multiplexer input "1" connected to one of the second terminals (SRIs) for external input connection, and a multiplexer output connected to the input of the second scan chain (130).

Regarding Claim 5, Motika discloses a switching arrangement ("mode select" signal of select register 142) to selectively connect the output end of the first scan chain (128) to the input end of the second scan chain (130), the input end and the output end of the second scan chain (130) to the second terminals (SRIs).

Regarding Claims 6 and 7, Motika discloses a compression logic, which is multiple input signature register (MISR) 16 receives signals from the output ends of the

plurality of scan chains (128, 130, 132, 134, 136) and produces one compressed output (SIGNAL OUT) Figure 2, at the compression logic output terminal.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al. (US 5983380).

Regarding Claim 4, Motika does not disclose a gate connected between the output end of the second scan chain of one of each pair of scan chains and one of the plurality of second terminals to selectively connect, in a second state, the output end of each second scan chain to one of the plurality of second terminals. However, Motika selectively connects with ("mode select" signal of select register 142), the output end of the second scan chain (130) to the input of MUX corresponding to scan chain 132, which is connected to the input of multiple input signature register (MISR) of the compression logic for test verification. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use configuration, as

taught by Motika, for the purpose of verifying each scan chain output, since the design configuration of Motika uses less components.

Claims 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Motika et al. (US 5983380) in view of Rajski et al. (US 6557129).

Regarding Claim 10, Motika discloses a semiconductor integrated circuit device under test (DUT) 14 having a test scan arrangement, Figures 1 and 2, comprising:

A plurality of scan chains (128, 130, 132, 134, 136) each having an input end and an output end and being arranged in pairs (128, 130) as first scan chain (128) and a second scan chain (130).

Compression logic multiple input signature register (MISR) 16 having a plurality of inputs and one output, where the plurality of inputs are connected to the output ends of the plurality of scan chains (128, 130, 132, 134, 136), and where the output is connected to the compression logic output terminal of the semiconductor integrated circuit (14) for external connection, as a (SIGNAL OUT) Figure 2.

Regarding Claims 8-10, Motika does not disclose compression logic comprising an XOR tree arranged on each block each having an XOR tree output, and a further XOR tree arranged to receive the XOR tree outputs on a plurality of connected blocks. However, Rajski et al. (US 6557129), in an analogous art, discloses a method and apparatus for selectively compacting test responses used in testing of integrated circuits, including a selective compactor 42 comprising Exclusive-OR (XOR) tree coupled to multiple scan chains 44 within a circuit under test, Figure 8. It would have

been obvious to a person having ordinary skill in the art at the time the invention was made to replace the multiple input signature register (MISR) of Motika with the Exclusive-OR (XOR) tree of Rajski, for the purpose of compressing the test responses from the scan chains, since spatial compactors provide design flexibility in customizing for a given circuit under test by limiting the number of their parallel inputs to reduce the error masking aliasing phenomenon.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James C Kerveros whose telephone number is (703) 305-1081. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4900.

Date:8 January 2004
File: Non-Final Rejection

U.S. PATENT OFFICE
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James C Kerveros
Examiner
Art Unit 2133

By: _____

Gregory J. Lamarre
for

Albert DeCady
Primary Examiner